SUBMICRON GATE INDIUM GALLIUM ARSENIDE MICROWAVE POWER TRANSISTORS

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ABSTRACT

Depletion mode InGaAs microwave power MISFETs with 0.7 um gate lengths and 0.2 mm gate widths have been fabricated using an epitaxial process. The devices employed a plasma deposited silicon dioxide gate insulator. The rf power performance at 18 GHz is presented. An output power density of 0.92 W/mm with a corresponding power gain and power-added efficiency of 3.2 dB and 29%, respectively, was obtained. This is the highest output power density obtained for an InGaAs based transistor on InP at K-band.

INTRODUCTION

Indium gallium arsenide (InGaAs) is a promising electronic material for high frequency applications. $In_{0.53}Ga_{0.47}As$ lattice matched to semi-insulating (SI) indium phosphide (InP) has higher low field mobility (12000 cm^2/V sec), peak electron velocity (3 x 10^7 cm/sec), and intervalley separation (0.55 eV) than InP or gallium arsenide (GaAs) (1). Metal-insulator-semiconductor field-effect transistors (MISFETs) fabricated on this semiconductor are, thus, expected to provide superior microwave performance compared to InP MISFETs. However, because InGaAs has lower ionization coefficients and a lower breakdown field than InP, high frequency device operation may be attained at the expense of reduced power output.

Recently, InGaAs MISFETs with 1 u m gate lengths have demonstrated an output power greater than 1 W at 9.7 GHz (2). An output power density of 1.07 W/mm of gate width was obtained with a corresponding power gain and power-added efficiency of 4.3 dB and 38%, respectively, at an input power of 26 dBm. In addition, excellent output power stability was demonstrated. Over 24 hours of continuous operation, output power was stable to within 1.2%

There have been very few reports of rf power measurements on InGaAs MISFETs at higher frequencies. Ion-implanted InGaAs MISFETs with 1 u m gate lengths have demonstrated output power densities of 0.40 W/mm and 0.27 W/mm with corresponding power-added efficiencies of25% and 19% at 10 GHz and 12 GHz, respectively (3). InGaAs power MISFETs with 1 um gate lengths have also demonstrated microwave performance in the frequency range from 12 GHz to 32.5 GHz (4). Output power densities of 0.76 W/mm 0.74 W/mm, and 0.20 W/mm have been obtained at 12 GHz, 20 GHz, and 32 GHz, respectively. The corresponding power-added efficiencies were 40%, 26%, and 7%. Recently, the wide-band microwave power performance of InGaAs MISFET amplifiers has been reported (5). Output power densities of 0.41 W/mm and 0.47 W/mm with corresponding power-added efficiencies of 33+ - 3% and 30+ - 3%, respectively, were obtained over the 7 - 11 GHz band. In addition, an output power density of 0.39 W/mm with 29+ - 4% power-added efficiency was obtained over the 6 - 12 GHz band.

This paper reports on the fabrication of 0.7 u m gate length depletion mode InGaAs MISFETs using an epitaxial process. The rf power performance at 18 GHz is presented. This is the first report of rf power measurements on InGaAs MISFETs with submicron gate lengths.

EXPERIMENTAL

The InGaAs MISFETs were fabricated on layers grown lattice matched on semi-insulating (SI) InP substrates using metal organic chemical vapor deposition (MOCVD). The thicknesses of the InGaAs layer and InP buffer layer were 0.3 u m and 0.2 u m, respectively. The InP layer was grown unintentionally doped while the InGaAs layer was doped to a level of 2-3 x 10^{17} cm^{-3}.

For the InGaAs MISFET fabrication, the samples were initially cleaned by first degreasing in acetone and methanol followed by a DI water rinse. The samples were then dipped for 15 sec in a 10:1 H_2O:HF solution followed by a DI water rinse and then blown dry in nitrogen. After the initial clean, a mesa etch was performed using a 1:1:38 H_2SO_4:H_2O_2:H_2O solution in order to define the device active area. Source/drain ohmic contacts were then defined by evaporating Au/Ge 12 wt.% eutectic and Au to a thickness of 1600 A and 1400 A, respectively, and using a liftoff process. Ohmic contacts were obtained by alloying for 5 min at 400 C in forming gas (10% H_2/N_2). The gate region was then chemically recessed using a 1:1:100 H_2SO_4:H_2O_2:H_2O solution.

After stripping the photoresist, the wafer was again cleaned and a silicon dioxide gate insulator was plasma deposited to a thickness of about 500 A (6). The films were deposited using a Technics

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PlanarEtch IIA plasma system modified for 13.56 MHz operation. The silicon dioxide films were deposited at 350 mTorr and 250 C using a 50 W plasma. The SiH_4 and N_2O flow rates were 19 sccm and 55 sccm, respectively. The gate insulators were subsequently annealed at 300 C for 30 min in hydrogen. The mesa area was then planarized by evaporating silicon dioxide to a thickness of 3500 A and using a liftoff process. The purpose of the e-beam oxide planarization step was to facilitate submicron gate length definition in the subsequent photolithographic step.

The gate metal was then defined by evaporating Ti and Au to a thickness of 200 A and 4500 A, respectively, and using a liftoff process. Finally, source/drain oxide windows were opened and a Au overlayer was deposited to a thickness of 4500 A using a liftoff process. The Au overlayer assisted the current handling of the devices and facilitated wire bonding to the drain regions.

The InGaAs MISFETs were prepared for rf packaging by first thinning the backside using a (10:1:1) $HCl:HNO_3:H_2O$ solution to improve thermal resistance and then scribing the sample into individual MISFETs. Backside metalization was then performed to aid heat dissipation of the MISFETs by evaporating Ti and Au to a thickness of 200 A and 4500 A, respectively. The completed MISFETs were then packaged and wire bonded for microwave characterization at 18 GHz.

RESULTS

The completed InGaAs MISFETs had 2 parallel gate gingers with individual gate widths of 100 um. The individual gate finger width was limited to the above values in order to avoid possible gain degradation associated with larger gate widths (7). The total gate width was 0.2 mm. The separation between the gate fingers was 114 um. The large spacing between the gate fingers was necessary in order to facilitate wire bonding to the individual drain regions. The source/drain contact spacing was 5 um and the length of the gate recess was 1 um. The device gate length was 0.7 um.

The device saturation current density was about 500 mA/mm of gate width. The device transconductance was typically about 70-80 mS/mm. The devices had typical source-drain breakdown voltages of 6 - 8 V. The gate-drain and gate-source breakdown voltages were typically greater than 20 V.

For the rf power measurements, the device was mounted on a test fixture using silver epoxy and subsequently wire bonded. The test fixture consisted of input and output microstrip circuits applied to a gold-plated brass block using a swear soldering technique. The microstrip circuits contained a rf choke for applying dc bias while chip capacitors were used as dc blocks across microstrip gaps. Electrical connections between the test fixture microstrip and measurement system were made using 2.4 mm coax to microstrip launchers. Impedence matching was done empirically using external metal stubs close to the transistor. The details of the test fixture have been described previously (8).

Figure 1 shows the output power and power-added efficiency as a function of input power from 12 dBm to 16.5 dBm for a 0.7 um gate length InGaAs MISFET with a total gate width of 0.2 mm. The measurements were performed at a frequency of 18 GHz using a gate-source bias of 0 V and a drain-source bias of 4.0 V. The linear gain was about 4.4 dB. An output power density of 0.44 W/mm of gate width was obtained with a corresponding power gain and power-added efficiency of 3.0 dB and 23%, respectively, at an input power of 16.5 dBm.

The gain compression curve obtained for input powers from 11 dBm to 20 dBm at gate-source and drain-source biases of -1.8 V and 6.8 V, respectively, is shown in Figure 2. The linear gain was about 6.2 dB. An output power density of 0.92 W/mm was obtained at an input power of 19.5 dBm. The corresponding gain and power-added efficiency were 3.2 dB and 29%, respectively. To our knowledge, this is the highest power density obtained for an InGaAs based transistor on InP at K-band. The highest power-added efficiency obtained was 32% with a corresponding power gain and output power density of 4.3 dB and 0.86 W/mm, respectively, at an input power of 18 dBm.

Of technological significance is the fact that the output power and drain bias current of these devices can be decreased and maintained for extended periods with negative gate bias at a fixed drain bias. The control of drain bias current through the use of a negative gate bias allowed the device output power to be optimized for the record output power density reported here. The short term (- 2 hours) output power stability of these devices appears excellent. It is expected that the long term output power stability will be similar to devices reported earlier (2).

SUMMARY

Depletion mode InGaAs MISFETs with 0.7 um gate lengths were fabricated using an epitaxial process. At 18 GHz, a 0.2 mm gate width device produced an output power density of 0.92 W/mm with a corresponding power gain and power-added efficiency of 3.2 dB and 29%, respectively. The highest power-added efficiency was 32% with a corresponding output power density of 0.86 W/mm and power gain of 4.3 dB. This is the first report of rf measurements on InGaAs MISFETs with submicron gate lengths. Further improvements are expected by optimizing the device structure. Presently, enhanced device performance is being investigated by reducing the device source/drain spacing.

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REFERENCES

(1) P. D. Gardner, S. Y. Narayan, and Y. H. Yun, "Characteristics of the Low - Temperature - Deposited SiO_2-$Ca_{0.43}In_{0.53}As$ Metal/Insulator/Semiconductor Interface", THIN SOLID FILMS, vol. 117, pp. 173-190 1984.

(2) G. A. Johnson, V. J. Kapoor, L. J. Messick, R. Nguyen, R. A. Stall, and M. McKee, "Indium Gallium Arsenide Microwave Power Transistors", IEEE TRANS. MICROWAVE THEORY TECH., to appear in 1991.

(3) P. D. Gardener, S. G. Liu, S. Y. Narayan, S. D. Colvin, J. P. Paczkowski, and D. R. Capewell, "Self-aligned gate GaInAs Microwave MISFETs", IEEE ELECTRON DEVICE LETT., vol. 7, pp. 363-364, 1986.

(4) P. D. Gardner, D. Bechtle, S. Y. Narayan, S. D. Colvin, and J. P. Paczkowski, "High Efficiency GaInAs Microwave MISFETs", IEEE ELECTRON DEVICE LETT., vol. 8, pp. 443-446, 1987.

(5) D. Bechtle, L. C. Upadhyayula, P. D. Gardner, and S. Y. Narayan, "Wide-band GaInAs MISFET Amplifiers", IEEE TRANS. MICROWAVE THEORY TECH., vol. 37, pp 1636-1638, 1989.

(6) M. Shokrani and V.J. Kapoor, "Gate Dielectric With Silicon Interfacial Layer on Indium Phosphide", J. ELECTROCHEM. SOCIETY, vol. 136, pp. 385C, 1989.

(7) M. D. Biedenbender, V. J. Kapoor, L. J. Messick, and R. Nguyen, "Ion-Implanted High Microwave Power Indium Phosphide Transistors", IEEE TRANS. MICROWAVE THEORY TECH. , vol. 37, pp. 1321-1326, 1989.

(8) M. D. Biedenbender, V. J. Kapoor, K. A. Shaulkhauser, L. J. Messick, R. Nguyen, D. Schmitz, H. Juergenson, "Submicron Gate InP Power MISFETs With Improved Output Power Density at 18 GHz and 20 GHz", IEEE TRANS MICROWAVE THEORY TECH., submitted for publication, February, 1991.

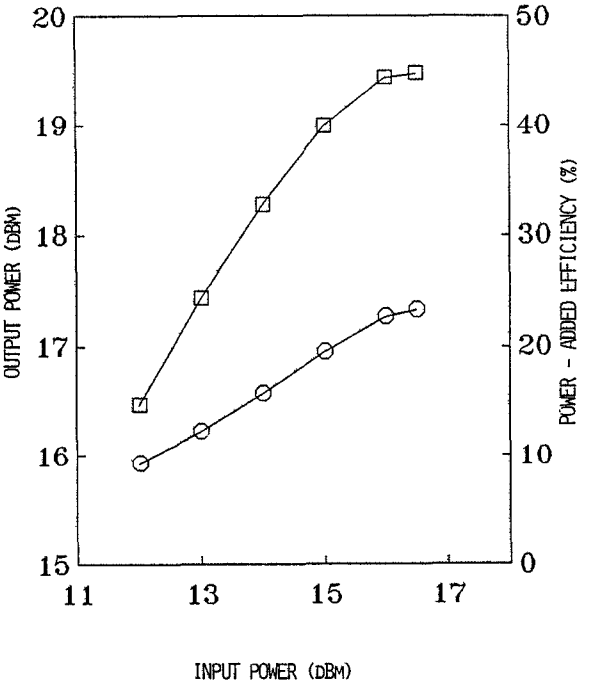

FIGURE 1

OUTPUT POWER, POWER-ADDED EFFICIENCY VS. INPUT POWER AT 18 GHz

(V_{DS} = 4.0 V, V_{GS} = 0 V)

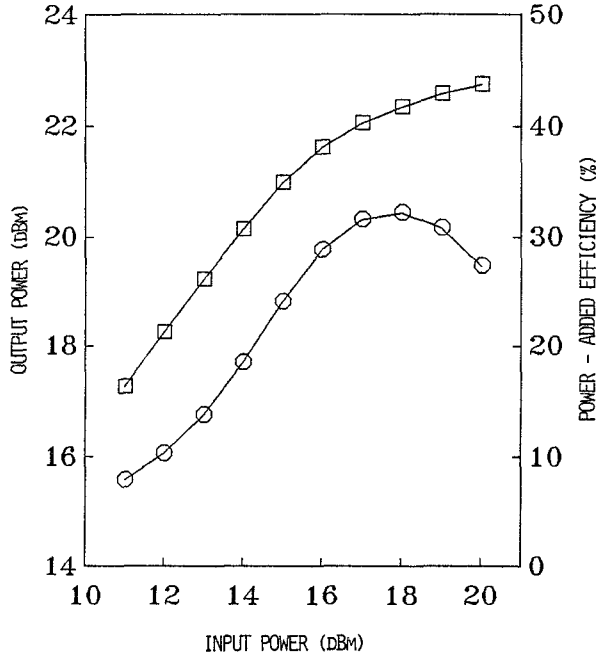

FIGURE 2

OUTPUT POWER, POWER-ADDED EFFICIENCY VS. INPUT POWER AT 18 GHZ

(V_{DS} = 6.8 V, V_{GS} = -1.8 V)